

New Patent Claims 1 to 8

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1. A semiconductor component having a semiconductor substrate and having an insulating layer produced on the semiconductor substrate and having a capacitance structure (K) produced in the insulating layer, which

5 - has a first substructure (T1a) which has a cohesive latticed metal region (G1a) which extends in a common plane (M1) parallel to the substrate surface such that it has common top and bottom surfaces which limit the latticed region (G1a) in each of its subregions from above and from below, and the latticed region (G1a) is electrically connected to a first connecting line, and

10 - which first substructure has electrically conductive regions (Pl<sub>a</sub>; KN) which are arranged in the cutouts in the latticed region (G1a) of the first substructure (T1a) at a distance from the edge regions of the cutouts in the plane (M1), and

15 the electrically conductive regions (Pl<sub>a</sub>; KN) are electrically connected to a second connecting line,

20 characterized in that the electrically conductive regions are metal plates (Pl<sub>a</sub> to Pl<sub>c</sub>) or node points (KN) between via connections.

2. The semiconductor component as claimed in claim 1, characterized in that

30 the capacitance structure (K) has a second substructure (T1b) which is produced parallel to and at a distance from the first substructure (T1a) and which has a metal, cohesive latticed region (G1b) which extends in a common plane (M2) parallel to the substrate surface

35 such that it has common top and bottom surfaces which limit the latticed region (G1b) in each of its subregions from above and below,

the first and second substructures (T1a, T1b) being electrically connected.

3. The semiconductor component as claimed in claim 2,  
5 characterized in that  
the second substructure (T1b) is of the same design as  
the first substructure (T1a), and the two substructures  
(T1a, T1b) are arranged offset from one another such  
that the electrically conductive regions (P1a) of the  
10 first substructure (T1a) are arranged vertically above  
the crossing points (KP) in the latticed region (G1b)  
of the second substructure (T1b), and the crossing  
points (KP) in the latticed region (G1a) of the first  
substructure (T1a) are arranged vertically above the  
15 electrically conductive regions (P1b) of the second  
substructure (T1b).

4. The semiconductor component as claimed in either  
of claims 2 and 3,  
20 characterized in that  
the crossing points (KP) in the latticed region (G1a)  
of the first substructure (T1a) are electrically  
connected to the electrically conductive regions (P1b)  
of the second substructure (T1b) which are arranged  
25 vertically below, and the electrically conductive  
regions (P1a) of the first substructure (T1a) are  
electrically connected to the crossing points (KP) in  
the latticed region (G1b) of the second substructure  
(T1b) which are arranged vertically below, by means of  
30 at least one respective via connection (V).

5. The semiconductor component as claimed in claim 2,  
characterized in that  
the latticed region (G1b) of the second substructure  
35 (T1b) is offset from the first substructure (T1a), so  
that the electrically conductive regions (P1a) of the  
first substructure (T1a) are arranged vertically above

the crossing points (KP) in the latticed region (G1b)  
of the second substructure (T1b).

6. The semiconductor component as claimed in claim 5,  
characterized in that  
the electrically conductive regions (Pla) of the first  
substructure (T1a) and the crossing points (KP) in the  
5 latticed region (G1b) of the second substructure (T1b)  
are electrically connected by means of one or more  
respective via connections (V).

7. The semiconductor component as claimed in one of  
10 claims 2 to 6,  
characterized in that  
a further substructure is in the form of a metal plate  
(MP) which is electrically connected to the crossing  
points (KP) in a latticed region (G1a; G1b) of a  
15 substructure (T1a, T1b) or to the electrically  
conductive regions (Pla, Plb) by means of one of more  
respective via connections (V).

8. The semiconductor component as claimed in one of  
20 the preceding claims,  
characterized in that  
the latticed regions (G1a to G1c) have at least two  
square or round cutouts.